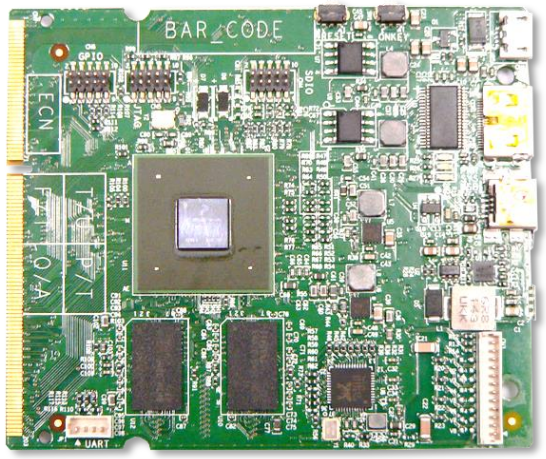
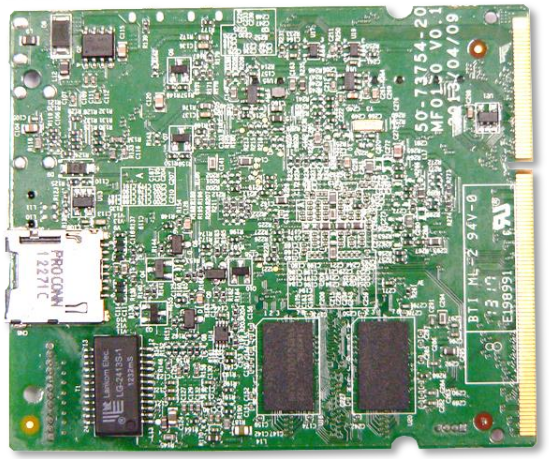
MF0100 SoM Board Specification Briefing

Mobile Division

Front View



Rear View



ARM Cortex™-A9 System-on-Module (SoM) Board

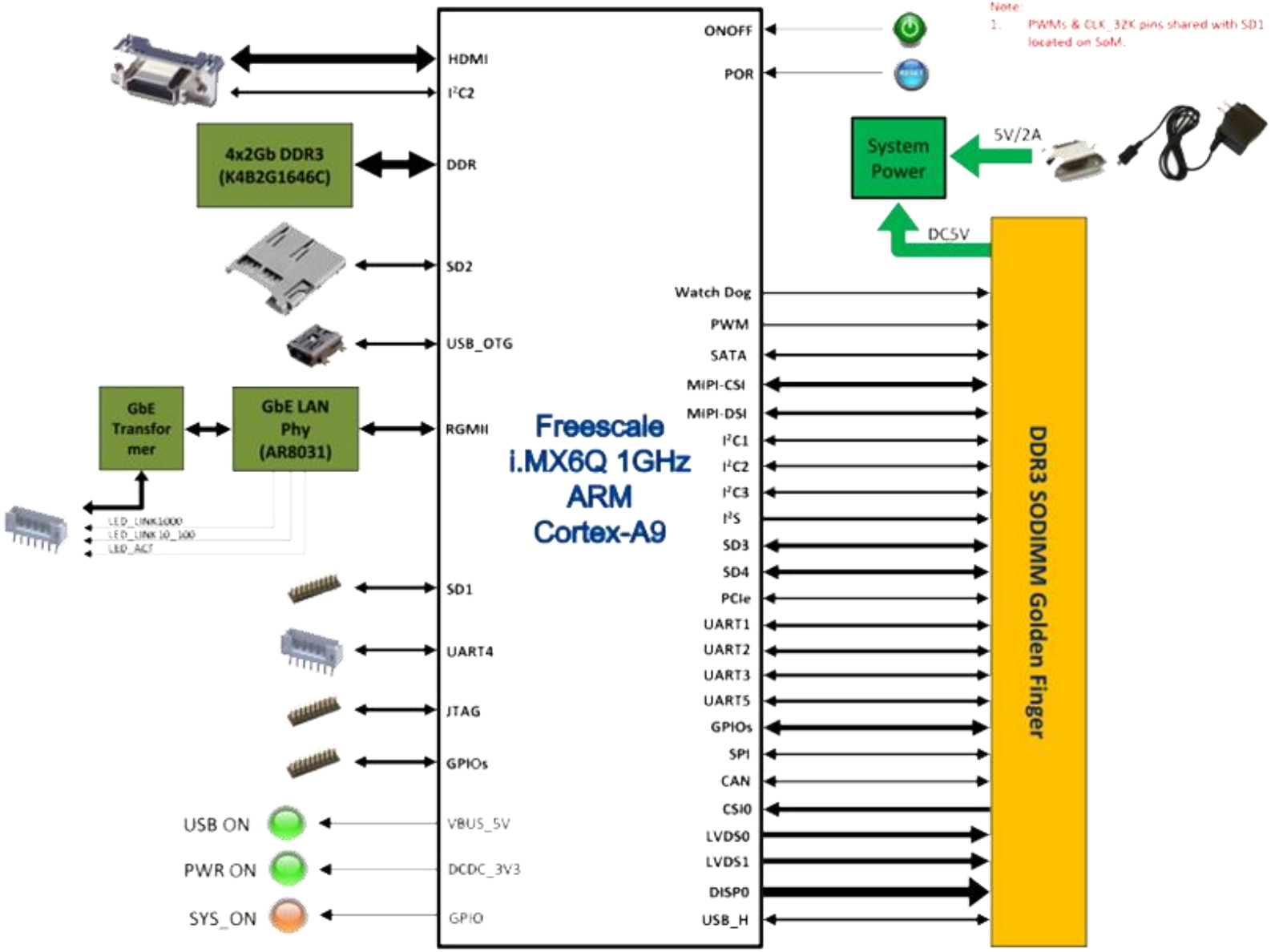
- Freescale i.MX6 Quad-Core or Dual Lite Processor
- 80x67.6 mm Small Form Factor
- Gigabit Ethernet Connectivity
- Cost-Effectiveness
- Function Expandability via a Standard SO-DIMM 204pin Interface
- Cost saving, Development time saving
- Supports Android, Linux

Android

freescale™ semiconductor

GbLAN | Card Slot | Mini HDMI | DDR 3 | Mini USB

MF0100 SoM Board Function Block Diagram



MF0100 SoM Board Specification

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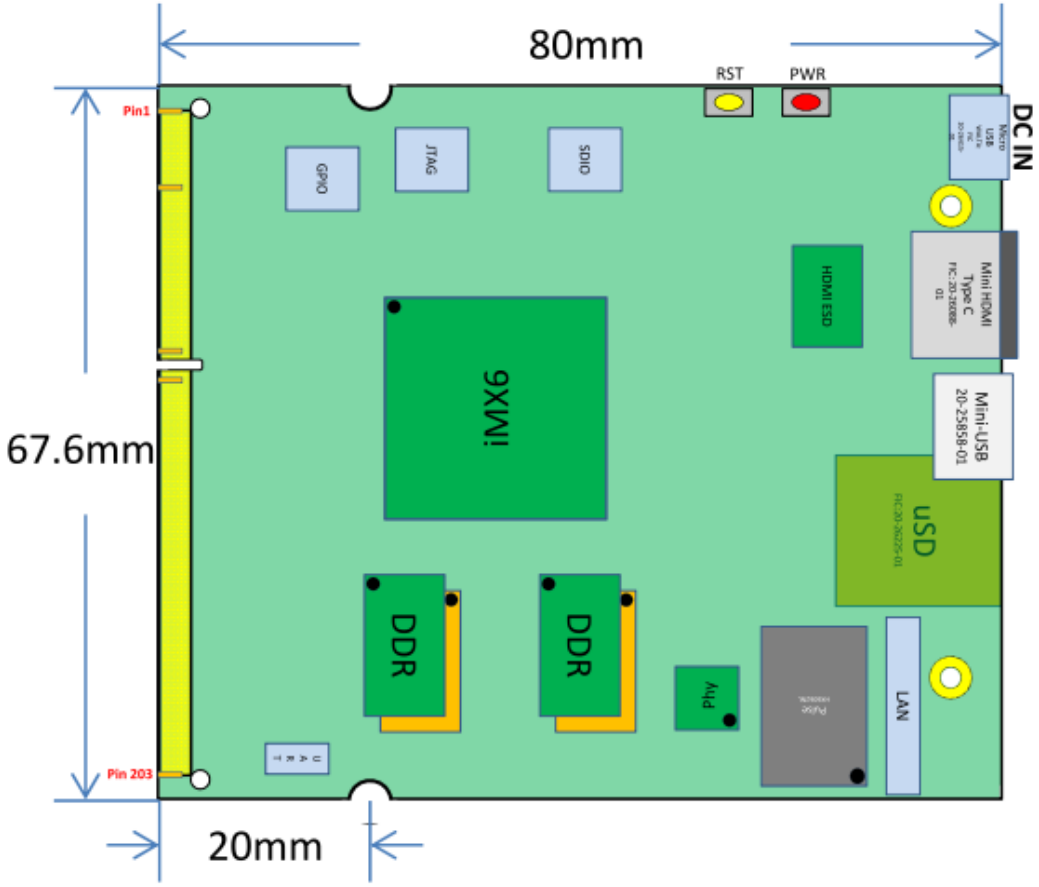
SoM Board	**CPU**	Freescale iMX6 Quad / Dual Lite*
	System RAM	1GB/512MB* DDR3
	HDMI	One (1) mini HDMI
	RTC	Included
	Power button	On/off
	Reset switch	HW reset
	UART	One (1) | 4 pin (Tx,Rx,3.3V,GND)
	JTAG	One (1) 2x5pin
	USB	One (1) mini-USB OTG
	Micro SD slot	One (1)
	Ethernet LAN	One (1) Gigabit LAN 1x 12pin for RJ45 cable
	SDIO	One (1) 2x5pin
	GPIO	One (1) 2x5pin
	Power in	One (1) Micro USB | 5V/2A
	LEDs	System Power on Local peripheral USB LED System boot status LED (SW control) Ethernet LED (via a Ethernet RJ45 connector cable)
	SO-DIMM Gold Finger	204pin Please refer to the next page for detail
	Dimension Size / Layer	67.6 x 80mm
	RoHS	Yes
Others	**Certification**	TBC
	Software Support	Linux, Android 4.0.4
Environment	**Operating Temperature**	0 ~60 degree (Commercial) -30~70 degree (Industrial grade per demand request)*
Package/Accessory	**Single brown box includes accessories:** Adaptor, QSG USB OTG, RJ45 cable (optional)	TBC

" * " Means optional SKU per request

i.MX6 SoM MF0100 PCB Placement
Size: 67.6 x 80 mm



MF0100 SoM Board Placement

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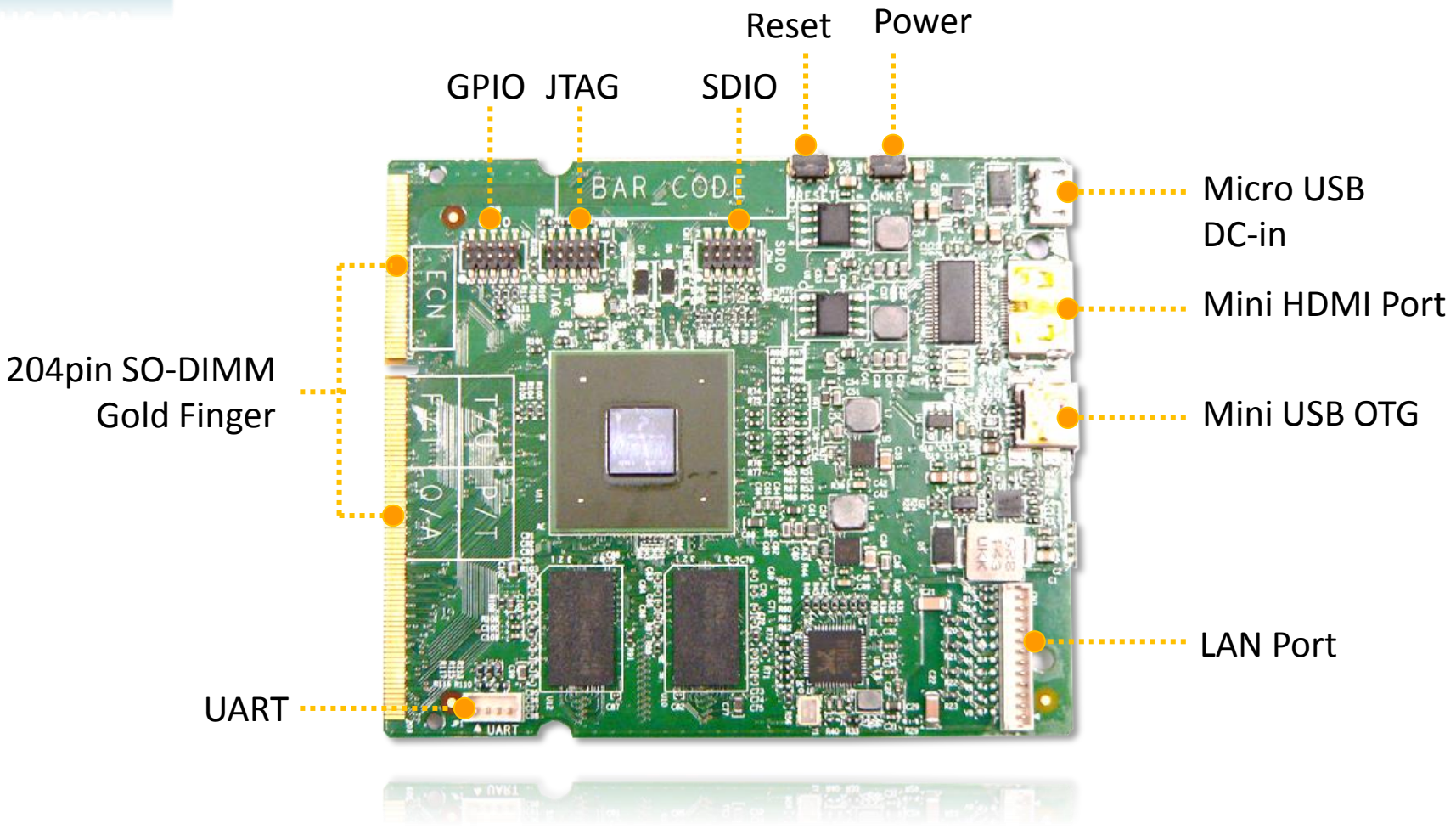
Front View



MF0100 SoM Board Placement

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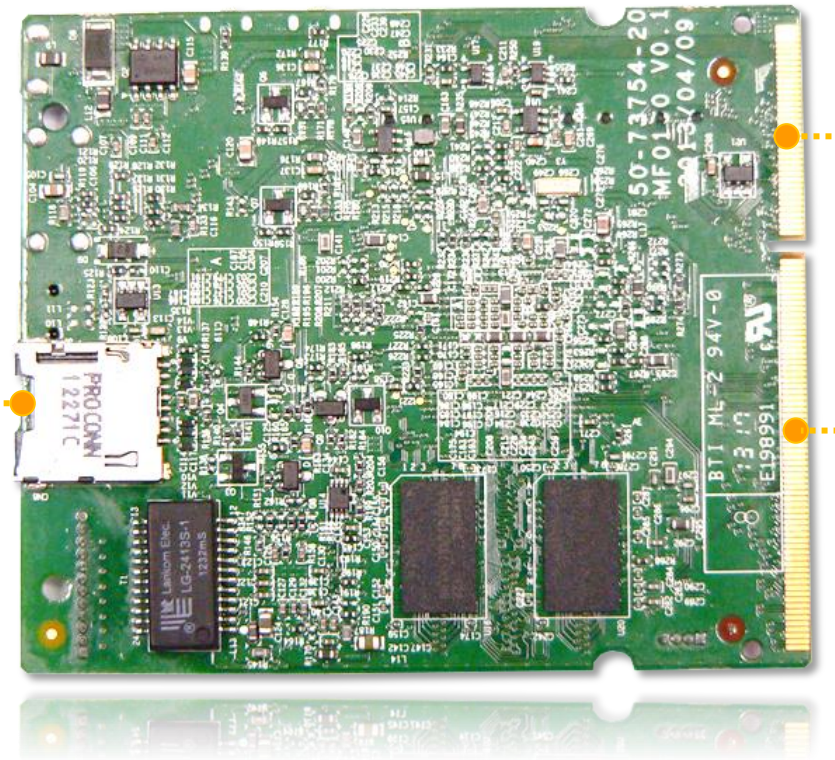
Rear View

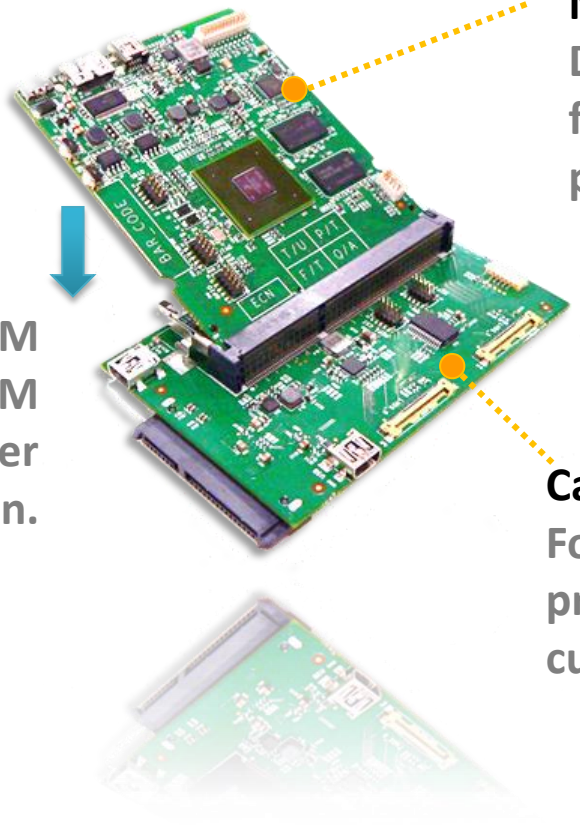


MF0100 SoM Board and Carrier Board Connecting Diagram

Mobile Division

MF0100 SoM Board

Designed by FIC to provide a flexible solution for fast OEM platform enablement.



Insert the 204pin SO-DIMM Gold Finger of MF0100 SoM board to connect the Carrier Board then push down.

Carrier Board

For extending the needs of product I/O functions per customer's request.

MF0100 SoM Board Function Pin Definition

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MF0100 SoM Pinout Description for DDR3 SODIMM Interface									
Pin	Signal	I/O	Description	Power Level	Pin	Signal	I/O	Description	Power Level
1	VCC5V	I	DC Input, Max: 5.5V, Norm: 5V, Min: 4.8V	5V	2	VCC5V	I	DC Input,Max:5.5V,Norm:5V,Min:4.8V	5V
3	VCC5V	I	DC Input, Max: 5.5V, Norm: 5V, Min: 4.8V	5V	4	VCC5V	I	DC Input,Max:5.5V,Norm:5V,Min:4.8V	5V
5	DISP0_DAT23	O	LCD Data Bit 23		6	VCC5V	I	DC Input,Max:5.5V,Norm:5V,Min:4.8V	5V
7	DISP0_DAT18	O	LCD Data Bit 18		8	DISP0_PWR_EN	O	LCD Power Enable/Disable	
9	DISP0_DAT20	O	LCD Data Bit 20		10	DISP0_DAT22	O	LCD Data Bit 22	
11	DISP0_DAT14	O	LCD Data Bit 14		12	DISP0_DAT21	O	LCD Data Bit 21	
13	DISP0_DAT17	O	LCD Data Bit 17		14	DISP0_DAT16	O	LCD Data Bit 16	
15	DISP0_DAT11	O	LCD Data Bit 11		16	DISP0_DAT19	O	LCD Data Bit 19	
17	DISP0_DAT9	O	LCD Data Bit 9		18	DISP0_DAT15	O	LCD Data Bit 15	
19	DISP0_DAT8	O	LCD Data Bit 8		20	DISP0_DAT12	O	LCD Data Bit 12	
21	DISP0_DAT7	O	LCD Data Bit 7		22	DISP0_DAT13	O	LCD Data Bit 13	
23	DISP0_DAT0	O	LCD Data Bit 0		24	DISP0_DAT6	O	LCD Data Bit 6	
25	DISP0_DAT5	O	LCD Data Bit 5		26	DISP0_RST_N	O	LCD Reset Signal	
27	DISP0_DAT1	O	LCD Data Bit 1		28	DISP0_DAT2	O	LCD Data Bit 2	
29	DISP0_DAT4	O	LCD Data Bit 4		30	DISP0_DAT10	O	LCD Data Bit 10	
31	DISP0_HSYNC	O	LCD Horizontal Synchronization		32	DISP0_DAT3	O	LCD Data Bit 3	
33	GND		Ground		34	DISP0_DRDY	O	LCD Data Ready	
35	DISP0_CLK	O	LCD Pixel Clock		36	DISP0_VSYNC	O	LCD Vertical Synchronization	
37	GND		Ground		38	SPI_MOSI	O	Serial Peripheral Interface Master Output; Slave	
39	UART2_CTS	I	Clear To Send		40	SPI_MISO	I	Serial Peripheral Interface Master Input; Slave	
41	UART2_RXD	I	Serial Data Receive		42	SPI_SCLK	O	Serial Peripheral Interface Clock	
43	UART2_TXD	O	Serial Data Transmit		44	SPI_SEL	O	Serial Peripheral Interface Chip Select	
45	UART2_RTS	O	Request To Send		46	UART3_CTS	I	Clear To Send	
47	MX6_ONOFF	I	System ON/OFF & Suspend/Wake-up Control, Active		48	UART3_RXD	I	Serial Data Receive	
49	POR_B	O	Power ON Reset, Active Low		50	UART3_TXD	O	Serial Data Transmit	
51	GPIO3_17	I/O	General Purpose I/O	3.3V	52	UART3_RTS	O	Request To Send	
53	USB_H1_OC	I	USB VBUS Power Over-Current Flag		54	PWM3	O	Pulse Width Modulator 1 (Shared Pin with	
55	USB_H1_PWR_EN	O	USB VBUS Power Enable/Disable		56	SD4_DATA7	I/O	SD Data7, for 8 bit mode	
57	USB_VBUS	O	USB Host Power Input, Max:5.25V, Norm:5V, Min:4.4V	5V	58	SD4_DATA4	I/O	SD Data4, for 8 bit mode	
59	USB_H1_DN	I/O	USB Host Negative Data Lane		60	SD4_DATA0	I/O	SD Data0, for 1/4/8 bit Mode	
61	USB_H1_DP	I/O	USB Host Postive Data Lane		62	SD4_DATA2	I/O	SD Data2, for 4/8 bit Mode or Read Wait	
63	GND		Ground		64	BOOT_SEL	I	Boot Device Select	
65	UART1_CTS	I	Clear To Send		66	SD4_CLK	O	SD Clock for MMC/SD/SDIO	
67	UART1_RTS	O	Request To Send		68	GND		Ground	
69	PWM1	O	Pulse Width Modulator 1 (Shared Pin with SD1_DAT3)		70	SD4_DATA6	I/O	SD Data6, for 8 bit mode	
71	GPIO2_5	I/O	General Purpose I/O	3.3V	72	SD4_DATA3	I/O	SD Data3, for 4/8 bit mode	
73	GPIO2_0	O	General Purpose I/O	3.3V	74	SD4_DATA5	I/O	SD Data5, for 8 bit mode	
75	GPIO2_4	I/O	General Purpose I/O	3.3V	76	SD4_DATA1	I/O	SD Data1, for 4/8 bit Mode	
77	GPIO6_15	I/O	General Purpose I/O	3.3V	78	SD4_CMD	I/O	SD Command Line	
79	GPIO6_14	I/O	General Purpose I/O	3.3V	80	GPIO6_7	I/O	General Purpose I/O	
81	GPIO6_10	I/O	General Purpose I/O	3.3V	82	GPIO6_11	I/O	General Purpose I/O	

MF0100 SoM Board Function Pin Definition

Mobile Division

83	SYS_ON_OFF_CTL	O	Auxiliary System ON/OFF Control		84	GND		Ground	
85	GPIO6_16	I/O	General Purpose I/O	3.3V	86	SATA_RXP	I	SATA Postive Receive Data Lane	
87	GPIO6_9	I/O	General Purpose I/O	3.3V	88	SATA_RXN	I	SATA Negative Receive Data Lane	
89	GPIO6_8	I/O	General Purpose I/O	3.3V	90	GND		Ground	
91	SD3_WP	I	SD Card Write Protect Detect		92	SATA_TXN	O	SATA Negative Transmit Data Lane	
93	SD3_CD_B	I	SD Card Detection Pin for MMC/SD		94	SATA_TXP	O	SATA Postive Transmit Data Lane	
95	SD3_DATA2	I/O	SD Data2, for 4/8 bit Mode or Read Wait		96	GND		Ground	
97	SD3_DATA3	I/O	SD Data3, for 4/8 bit mode		98	CSI_D0P	I/O	MIPI Camera Serial Interface Postive Data Lane 0	
99	GND		Ground		100	CSI_D0M	I/O	MIPI Camera Serial Interface Negative Data Lane 0	
101	SD3_CLK	O	SD Clock for MMC/SD/SDIO		102	GND		Ground	
103	GND		Ground		104	CSI_CLK0P	O	MIPI Camera Serial Interface Postive Clock Lane	
105	SD3_DATA0	I/O	SD Data0, for 1/4/8 bit Mode		106	CSI_CLK0M	O	MIPI Camera Serial Interface Negative Clock Lane	
107	SD3_DATA4	I/O	SD Data4, for 8 bit mode		108	GND		Ground	
109	SD3_DATA6	I/O	SD Data6, for 8 bit mode		110	CSI_D2P	I/O	MIPI Camera Serial Interface Postive Data Lane 2	
111	SD3_DATA1	I/O	SD Data1, for 4/8 bit Mode		112	CSI_D2M	I/O	MIPI Camera Serial Interface Negative Data Lane 2	
113	SD3_DATA7	I/O	SD Data7, for 8 bit mode		114	GND		Ground	
115	SD3_DATA5	I/O	SD Data5, for 8 bit mode		116	CSI_D3M	I/O	MIPI Camera Serial Interface Negative Data Lane 3	
117	SD3_CMD	I/O	SD Command Line		118	CSI_D3P	I/O	MIPI Camera Serial Interface Postive Data Lane 3	
119	GND		Ground		120	GND		Ground	
121	PCIe_CREFCLKM	O	PCIe Negative Reference Clock Lane		122	CSI_D1P	I/O	MIPI Camera Serial Interface Postive Data Lane 1	
123	PCIe_CREFCLKP	O	PCIe Postive Reference Clock Lane		124	CSI_D1M	I/O	MIPI Camera Serial Interface Negative Data Lane 1	
125	GND		Ground		126	GND		Ground	
127	PCIe_TXM	O	PCIe Negative Transmit Data Lane		128	DSI_CLK0P	O	MIPI Display Serial Interface Postive Clock Lane	
129	PCIe_TXP	O	PCIe Postive Transmit Data Lane		130	DSI_CLK0M	O	MIPI Display Serial Interface Negative Clock Lane	
131	GND		Ground		132	GND		Ground	
133	PCIe_RXP	I	PCIe Negative Postive Data Lane		134	DSI_D0M	I/O	MIPI Display Serial Interface Negative Data Lane 0	
135	PCIe_RXM	I	PCIe Negative Receive Data Lane		136	DSI_D0P	I/O	MIPI Display Serial Interface Postive Data Lane 0	
137	GND		Ground		138	GND		Ground	
139	I2S_LRCLK	I/O	I2S Frame Clock		140	DSI_D1M	I/O	MIPI Display Serial Interface Negative Data Lane 1	
141	I2S_SCLK	O	I2S bit Clock		142	DSI_D1P	I/O	MIPI Display Serial Interface Postive Data Lane 1	
143	I2S_DIN	I	I2S Data Input		144	GND		Ground	
145	I2S_DOUT	O	I2S Data Output		146	CAN1_STBY	O	CAN Bus Standby Mode Control	
147	I2C1_SDA	I/O	I2C Serial Data	3.3V	148	CAN1_RXD	I	CAN Bus Data Receive	
149	I2C1_SCL	O	I2C Serial Clock	3.3V	150	CAN1_TXD	O	CAN Bus Data Transmit	
151	UART1_RXD	I	Serial Data Receive		152	CSI0_DAT19	I/O	Camera Sensor Interface Data bit 7	
153	UART1_TXD	O	Serial Data Transmit		154	CSI0_DAT17	I/O	Camera Sensor Interface Data bit 5	
155	PCIE_WAKE_B	I	PCIe Wake -Up Event		156	CSI0_DAT16	I/O	Camera Sensor Interface Data bit 4	
157	I2C3_SDA	I/O	I2C Serial Data	3.3V	158	CSI0_DAT15	I/O	Camera Sensor Interface Data bit 3	
159	I2C3_SCL	O	I2C Serial Clock	3.3V	160	CSI0_DAT13	I/O	Camera Sensor Interface Data bit 1	
161	WDOG_B	O	Watch-Dog Signal Output		162	CSI0_DAT12	I/O	Camera Sensor Interface Data bit 0	
163	I2C2_SCL	O	I2C Serial Clock (HDMI)	3.3V	164	CSI0_DAT14	I/O	Camera Sensor Interface Data bit 2	

165	I2C2_SDA	I/O	I2C Serial Data (HDMI)	3.3V	166	CSI0_DAT18	I/O	Camera Sensor Interface Data bit 6	
167	UART5_RTS	O	Request To Send		168	CSI0_HSYNC	O	Camera Sensor Interface Horizontal Synchronization	
169	UART5_RXD	I	Serial Data Receive		170	CSI0_VSYNC	O	Camera Sensor Interface Vertical Synchronization	
171	UART5_TXD	O	Serial Data Transmit		172	GND		Ground	
173	UART5_CTS	I	Clear To Send		174	CSI0_PCLK	O	Camera Sensor Interface Pixel Clock	
175	GND		Ground		176	GND		Ground	
177	LVDS0_TX2_P	O	Positive LVDS Data Lane 2		178	LVDS0_TX0_P	O	Positive LVDS Data Lane 0	
179	LVDS0_TX2_N	O	Negative LVDS Data Lane 2		180	LVDS0_TX0_N	O	Negative LVDS Data Lane 0	
181	GND		Ground		182	GND		Ground	
183	LVDS0_TX1_P	O	Positive LVDS Data Lane 1		184	LVDS0_TX3_P	O	Positive LVDS Data Lane 3	
185	LVDS0_TX1_N	O	Negative LVDS Data Lane 1		186	LVDS0_TX3_N	O	Negative LVDS Data Lane 3	
187	GND		Ground		188	GND		Ground	
189	LVDS1_TX0_N	O	Negative LVDS Data Lane 0		190	LVDS0_CLK_P	O	Positive LVDS Clock Lane	
191	LVDS1_TX0_P	O	Positive LVDS Data Lane 0		192	LVDS0_CLK_N	O	Negative LVDS Clock Lane	
193	GND		Ground		194	GND		Ground	
195	LVDS1_TX1_P	O	Positive LVDS Data Lane 1		196	LVDS1_CLK_P	O	Positive LVDS Clock Lane	
197	LVDS1_TX1_N	O	Negative LVDS Data Lane 1		198	LVDS1_CLK_N	O	Negative LVDS Clock Lane	
199	GND		Ground		200	GND		Ground	
201	LVDS1_TX2_N	O	Negative LVDS Data Lane 2		202	LVDS1_TX3_P	O	Positive LVDS Data Lane 3	
203	LVDS1_TX2_P	O	Positive LVDS Data Lane 2		204	LVDS1_TX3_N	O	Negative LVDS Data Lane 3	